REMARKS

Claims 1-7, 9, 10 and 13-19 are pending. Claims 8, 11, 12 and 20-23 are canceled. Claims 1 and 13-17 have been amended. Claim 1 has been amended to address an informality in the claim. Claims 13-17 have been amended to simplify the issues presented for appeal. No new matter has been introduced.

The Examiner is thanked for entering the Amendment of January 26, 2009 for purposes of appeal.

The Examiner rejected claims 13, 14, 16 and 18-22 under 35 USC Section 102(b) as anticipated by U.S. Patent Publication No. 2002/0055979 by Koch. The Examiner rejected claims 1-7, 9, 10, 15 and 17 under 35 U.S.C. Section 103(a) as obvious over Koch in view of U.S. Patent No. 6,775,717 issued to Tang. The Examiner's rejections are respectfully traversed.

With regard to claims 1-7, 9 and 10, independent claim 1 recites, "the first programmable unit and the second programmable unit each comprises: a direct access unit core; a first external direct memory access channel interface on the first clock; and a second external direct memory access channel interface on the second clock," and claims 2-7, 9 and 10 depend from claim 1. The Examiner points to access unit 51, DMA 41, interface 42, paragraphs 45, 48, 51 and 56 and Figure 4 of Koch as teaching programming elements for a programmable unit. The cited portions of Koch do not disclose two programmable units each of which has two external direct memory access channel interfaces, each on one of two clocks. The Examiner contends that two external DMA channels is taught by Tang. The Examiner admits that the combination of Koch and Tang does not disclose two programmable units each of which has two direct memory access channels interfaces one on each of two clocks. The Examiner contends it would have been obvious to make this additional modification after combining Koch and Tang, without citing an additional reference. Tang is directed to an arbitration system for a system with a common bus clock. Tang teaches arbitration and reduction in latency between completion of a first data transfer of a first DMA channel interface and the set up of a second data transfer of a second DMA channel interface on the same bus and the same clock. The motivation to which the Examiner points for making the additional modification is reducing the latency time between DMA transfers. This would seem to motivate, if anything, adding a second direct memory

access channel interface on a same clock, rather than motivating a second direct memory access channel interface on a different clock. In the Advisory Action, the Examiner fails to address Applicants' argument that the references, alone or in combination, do not disclose two programmable units each of which has two direct memory access channels interfaces one on each of two clocks. Accordingly, it is respectfully submitted that claims 1-7, 9 and 10 are not rendered obvious by Koch, alone or in combination with Tang, because the combination of Koch with Tang does not teach, disclose or motivate "the first programmable unit and the second programmable unit each comprises: a direct access unit core; a first external direct memory access channel interface on the first clock; and a second external direct memory access channel interface on the second clock," as recited. It is noted that the Examiner commented that the previous amendment was attacking the references separately. It is respectfully submitted that the previous and current amendments argue that the suggested combination of references fails to disclose every element recited in the claims, which is required to establish a prima facie case of obviousness.

Independent claim 13, as amended recites, "the first bi-directional channel comprises: a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock; and a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and a second bi-directional channel ... [comprising] a second external channel of the first DMA unit to operate on the first processor clock; and a second external channel of the second DMA unit to operate on the second processor clock." Claims 14-19 depend from claim 13. Koch, alone or in combination with Tang, does not teach, suggest, motivate or otherwise render obvious a system comprising: a first bi-directional channel having a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock and a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock; and a second bi-directional channel having a second external channel of the first DMA unit to operate on the first processor clock and a second external channel of the second DMA unit to operate on

the second processor clock. Thus, claims 13-19 are not anticipated or rendered obvious by Koch, alone or in combination with Tang.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/Timothy L. Boller/
Timothy L. Boller
Registration No. 47,435

TLB:

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

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